

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:
a plurality bonding pads arranged along at least one side of a least one semiconductor chip embedded in the semiconductor integrated circuit device;
at least one inspection pad on another side of the semiconductor chip; and
a corresponding connection wire, which is laid outside an input/output buffer area of the chip for each of said bonding pads, for connecting said each bonding pad with the inspection pad.
2. The semiconductor integrated circuit device as claimed in claim 1, wherein each of a plurality of semiconductor chips of said semiconductor integrated circuit device being arranged on a wafer so as to arrange the sides with the inspection pads of said chips in parallel.
3. The semiconductor integrated circuit device as claimed in claim 1, wherein at least one connection wire is laid inside the input/output buffer area.
4. The semiconductor integrated circuit device as claimed in claim 1, wherein each said connection wire has the same length.
5. The semiconductor integrated circuit device as claimed in claim 1, wherein:
the inspection pads and the connection wires are laid in a scribing area;

the inspection pads and the bonding pads are arranged in a row or zigzag such that the inspection pads and the connection wires are to be removed from the semiconductor integrated circuit device when the semiconductor integrated circuit device is cut off from a wafer at the scribing area after the semiconductor integrated circuit device is inspected with probe needles.

6. The semiconductor integrated circuit device as claimed in claim 1, wherein:
the connection wires are laid in at least one wiring layer; and
GND lines are laid between the connection wires or at least one GND layer is formed between the wiring layers.
7. The semiconductor integrated circuit device as claimed in claim 1, wherein an electrostatic discharge protection element is disposed in the vicinity of each said inspection pad.
8. A semiconductor integrated circuit package having leads on four sides, comprising:
a semiconductor integrated circuit device with bonding pads laid along one pair of opposite sides of the four sides; and
a table for supporting the semiconductor integrated circuit device,
wherein the bonding pads along the pair of opposite sides of the semiconductor integrated circuit device are connected with leads along the four sides of the package.
9. The package as claimed in claim 8, wherein the leads comprises:
first outer leads arranged along a first side of the package;
second outer leads arranged along a second side, perpendicular to the first side,

second inner leads corresponding to the second outer leads.

15. The package as claimed in claim 8, where the leads constitute the table for supporting.

16. The package as claimed in claim 8, wherein at least one electrostatic discharge protection element is provided for at least one of the pads.

17. The package as claimed in claim 9, wherein at least one of the second inner leads have tips arranged zigzag with respect to tips of the first inner leads.

18. The package as claimed in claim 9, wherein the second inner leads are connected to the second outer leads via wires outside of the semiconductor integrated circuit device and inside the package.

19. The package as claimed in claim 9, wherein each of the bonding pads is either connected to the inner leads with bonding wires, and the bonding wires are laid outside an input/output buffer area of the chip.

20. A semiconductor integrated circuit device, comprising:

a plurality bonding pads arranged along at least one side of a least one semiconductor chip embedded in the semiconductor integrated circuit device;

at least one inspection pad on another side of the semiconductor chip; and

a corresponding connection wire for each of said bonding pads for connecting said each bonding pad with the inspection pad,

wherein at least one of the bonding pads, the inspection pads and the connection wire is to be removed from the device when the device is cut off from a wafer.